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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/796,427	03/09/2004	Mou-Shiung Lin	MEG03-005	1870
7590 06/30/2005 STEPHEN B. ACKERMAN 28 DAVIS AVENUE POUGHKEEPSIE, NY 12603			EXAMINER LEWIS, MONICA	
			ART UNIT 2822	PAPER NUMBER

DATE MAILED: 06/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/796,427

Applicant(s)

LIN ET AL.

Examiner

Monica Lewis

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 30days MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 March 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-68 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☐ Claim(s) _____ is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☒ Claim(s) 1-68 are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

1. This action is in response to the application filed March 10, 2004.

Election/Restrictions

2. Restriction to one of the following inventions is required under 35 U.S.C. 121:
 - I. Claim 1-10 and 47-68, drawn to a semiconductor device with an integrated circuit, classified in class 257, subclass 703.
 - II. Claims 11-46, drawn to the method of fabricating a semiconductor device with an integrated circuit, classified in class 438, subclass 622.

Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). The product can be made by the following methods: a) the topmost passivation layer could be selectively deposited thereby eliminating the need to provide vias through the layer after the passivation layer is provided on the plurality of levels of interconnection lines and dielectric materials.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the

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application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143).

3. If the Applicant selects Invention I disclosed then application contains claims directed to the following patentably distinct species of the claimed invention:

Embodiment I (Claims 1-10), directed to a semiconductor device comprising a semiconductor house in and on a substrate, a plurality of levels of interconnection lines and interlevel dielectric materials overlying and connecting said semiconductor structures wherein a topmost level of said interconnection lines includes contact pads, a topmost passivation layer overlying said plurality of levels of interconnection lines and interlevel dielectric materials, a metal cap overlying each of said contact pads through an opening in said topmost passivation layer and a gold pad overlying said metal cap;

Embodiment II (Claims 47-55), directed to a semiconductor device comprising a semiconductor house in and on a substrate, a plurality of levels of interconnection lines and interlevel dielectric materials overlying and connecting said semiconductor structures, a topmost passivation layer overlying said plurality of levels of interconnection lines and interlevel dielectric materials, a metal cap overlying each of a topmost of said interconnection lines through an opening;

Embodiment III (Claims 56-60), directed to a semiconductor device formed on a semiconductor substrate, with an overlying interconnecting metallization structure connected to said devices and comprising a plurality of first metal lines, and having a passivation layer formed thereover, with first openings in said passivation layer to contact pads connected to said first metal lines, wherein said openings are as small as .1 μm , a metal cap on each of contact pads within each of first openings, a top metallization system formed over said passivation layer and said metal caps, connected to said metal caps and said interconnecting metallization structure, wherein said top metallization system comprises a plurality of top metal lines, in one or more layers, having a thickness substantially greater than said first metal lines;

Embodiment IV (Claims 61-64), directed to a semiconductor device, a semiconductor substrate, having at least one interconnect metal layer over said substrate, wherein the passivation layer comprises at least one passivation opening through which is exposed at least one top level metal contact point, a metal cap formed over said exposed at least one top level metal contact point, a passive component formed over said passivation layer; and

Embodiment V (Claims 65-68), directed to a semiconductor device, a semiconductor substrate, having at least one interconnect metal layer over said substrate, wherein the passivation layer comprises at least one passivation opening through which is exposed at least one top level metal contact point, a

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metal cap formed over said exposed at least one top level metal contact point, a passive component formed over said passivation layer.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, none are generic.

Applicant is advised that a reply to this requirement must include an identification of the species that is elected consonant with this requirement, and a listing of all claims readable thereon, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which are written in dependent form or otherwise include all the limitations of an allowed generic claim as provided by 37 CFR 1.141. If claims are added after the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a).

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 571-272-1838.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722 for regular and after final

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communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML

June 27, 2005



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